Amendment to the Claims:

This listing of claims will replace all versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An application-specific integrated circuit (ASIC), comprising:

switch circuitry for receiving a data frame and forwarding it to a predetermined port;

inspection circuitry for inspecting attributes of the data frame;

decision circuitry for instructing the switch circuitry to forward the data frame based on the attributes; and

a memory mapped interface accessible to a plurality of wireless access points in data communication with the ASIC;

wherein the memory mapped interface stores packets for the plurality of wireless access points and provides Media Access Control layer processors associated with the plurality of access points with access to the data frames;

wherein a data frame is stored in a memory area corresponding to a wireless access point for transmitting the packet, the data frame remaining in the memory area until after the data frame is transmitted by the wireless access point and an acknowledgement for the data frame is received by a Media Access Control processor associated with the wireless access point.

2. (Original) The integrated circuit of claim 1 wherein the inspection circuitry is configured to inspect for wireless attributes and wherein the decision circuitry is configured to block non-wireless data frames from wireless ports.

3. (Original) The integrated circuit of claim 1 wherein the inspection circuitry is configured to determine whether a data frame is of higher priority than another data frame, and wherein the decision circuitry is configured to grant precedence in forwarding to the higher priority data frame.

4. (Original) The integrated circuit of claim 3 further comprising a queue for prioritizing data frames, so as to provide quality of service.

5. (Original) The integrated circuit of claim 1 further comprising protocol conversion circuitry for translating the data frame between a first protocol and a second protocol.

6. (Original) The integrated circuit of claim 5 wherein the first protocol is an Ethernet network protocol and the second protocol is a wireless protocol.

7. (Canceled) The integrated circuit of claim 1 further comprising a memory map for storing and retrieving data frames in a memory according to a data frame's address.

8. (Original) The integrated circuit of claim 7 further comprising circuitry for selectively retrieving data frames based on priority.

9. (Original) The integrated circuit of claim 7 further comprising circuitry for translating data frames between a first protocol and a second protocol.

10. (Original) The integrated circuit of claim 9 wherein the first protocol is an Ethernet network protocol and the second protocol as a wireless protocol.

11. (Currently Amended) An network switch comprising:

a plurality of ports for connecting to a plurality of network devices, for exchanging data frames between at least some of the network devices;

a microprocessor-driven application-specific integrated circuit (ASIC) comprising

switch circuitry for receiving a data frame and forwarding it to a predetermined port;

inspection circuitry for inspecting attributes of the data frame;

decision circuitry for instructing the switch circuitry to forward the data frame based on the attributes;

a memory mapped interface accessible to a plurality of wireless access points in data communication with the ASIC;

wherein the memory mapped interface stores packets for the plurality of wireless access points and provides Media Access Control layer processors associated with the plurality of access points with access to the packets;

wherein a packet is stored in a memory area corresponding to a wireless access point for transmitting the packet, the packet remaining in the memory area until after the packet is transmitted by the wireless access point and an acknowledgement for the packet is received by a Media Access Control processor associated with the wireless access point.

12. (Original) The network switch of claim 11 wherein the inspection circuitry is configured to inspect for wireless attributes and wherein the decision circuitry is configured to block non-wireless data frames from wireless ports.

13. (Original) The network switch of claim 11 wherein the inspection circuitry is configured to determine whether a data frame is of higher priority than another data frame, and wherein the decision circuitry is configured to grant precedence in forwarding to the higher priority data frame.

14. (Original) The network switch of claim 13 further comprising a queue for prioritizing data frames, so as to provide quality of service.

15. (Original) The network switch of claim 11 further comprising protocol conversion circuitry for translating the data frame between a first protocol and a second protocol.

16. (Original) The network switch of claim 15 wherein the first protocol is an Ethernet network protocol and the second protocol is a wireless protocol.

17. (Original) The network switch of claim 11 further comprising a memory map for storing and retrieving data frames in a memory according to a data frame's address.

18. (Original) The network switch of claim 17 further comprising circuitry for selectively retrieving data frames based on priority.

19. (Original) The network switch of claim 17 further comprising circuitry for translating data frames between a first protocol and a second protocol.

20. (Canceled)

21. (New) The integrated circuit of claim 1, further comprising one of a group consisting of a core for 802.11 to 802.3 header stripping, a core for 802.11 to 802.3 encapsulation, a core for providing Message Integrity Check (MIC) hardware assistance, and radio client association tables.